Shuanghua Liu

Mobile: (+44) 7455959926 E-mail: peterliu20010523@gmail.com
Personal Website: https://www.shuanghualiu.com

EDUCATION

Imperial College London, *MEng Electrical and Electronic Engineering with Management* ***2019-Present***

- On target for First Class Honours.
- Relevant modules**:**Analysis and Design of Circuits, Digital and Computer Architecture, Programming for Engineers, Electronics Laboratory Skills, Electronics Design Project, Circuit and System, Power electronics and Power system, Signal and system, Artificial Intelligence, Analogue circuit design, Full custom IC circuit, High performance electronic, Advanced analogue signal processing

Cardiff Sixth Form College, UK, *A-Level graduated with A*A*A*A* ***2017-2019***

King Edward School Witley, UK ***2016-2017***

Academic Achievements: A Level A*A*A* in Mathematics, Further Mathematics and Physics, A in Economics, with full UMS in Mathematics and 599/600 UMS in Further Mathematics.

Obtained Awards: British Physics Olympiad Round 1 (Silver), UK Senior Math Challenge (Silver), UK Junior Math Challenge (Silver), China Mathematics, Physics, and Chemistry competitions (Secondary award for Mathematics).

WORK EXPERIENCE

Arm, Manchester **June- September *2022***

Hardware verification engineer

- Updating testbench for next generation SMMU(System Memory Management Unit)
- Implement performance logger to track time delay in different blocks
- Using verification tools like JasperGold and Questasim, also Universal Verification Methodology

Jiangsu Leike Defense Technology Co Ltd, China **August- September *2021***

Data Centre Engineer

- Built the Server group and SRS to do video streaming independently.
- Participated in transcoding RTSP to RTMP to push into the server, wrote the hardware monitoring program in C++ and sent it through MQTT channel.
- Deployed Kubernetes and Jenkins to manage virtualized systems and applications.

RESEARCH EXPERIENCE

Design a CMOS ISFET array with On-Chip Compressed Sensing ***2022***

- Using Iterative Curvelet Thresholding Basis with orthogonal matching pursuit algorithms to reconstruct the compressed data from ISFET array.
- Design a low-power low-noise ADC as a quantisation circuit and boost the frame rate while improve power efficiency.

Team Project to Build an autonomous Mars Rover ***2021***

- Integrated all parts together, which requires sufficient knowledge in command, control, vision, drive and power fields, as well as project management skill.
- Implemented the serial communication between FPGA, ESP32, ARDUINO NAVY and the power PCB. Strengthened technical capabilities in C++ ,C,Verilog, HTML, and JavaScript.

Team Project for CPU Architecture Design ***2020***

- Designed a CPU with Harvard architecture and ARMish architecture from scratch in Verilog.
- Implemented to achieve three benchmarks, Calculating Fibonacci numbers, Pseudo-random integers with a linear congruential generator, Traverse a linked list.

TECHNICAL SKILLS

- **Programming Skills:** Proficient in Verilog, Python, C++ and MATLAB
- **Software:** Altium, Cadence Virtuoso, JasperGold, Questasim
- **Language:** Fluent in English (CEFR Level C1), Latin (GCSE A*), Mandarin (Native)
- **Interests:** Saxophone, piano, photography